NR

Code No: A5701

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.Tech I Semester Examinations, October/November-2011
DIGITAL SYSTEM DESIGN
(VLSI STSTEM DESIGN)

Time: 3hours **Max. Marks: 60**

Answer any five questions
All questions carry equal marks
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1.a) Draw an ASM chart to design a control logic of a binary multiplier.
b) Realize the above design using MUX, decoder and D-type flip flops. [12]

2.a) Draw the general structure of a CPLD and explain how a logic function can be realized on CPLD with simple example.
b) Design a four-way traffic light controller that will keep traffic moving efficiently along two busy streets that intersect. Implement the controller using PALs. [12]

3.a) Using the path-sensitization method and Boolean difference method find the test vectors for SA0 fault on input line 1 and SA1 fault on the internal line 2 of the circuit shown in figure 1.

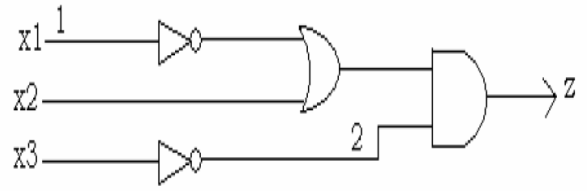

figure 1

b) Explain how Kohavi algorithm is useful in the detection of faults in digital circuits. [12]

4.a) Apply D-algorithm to detect SA0 fault at point 'h' in the given circuit shown in figure 2 and derive the test vectors.

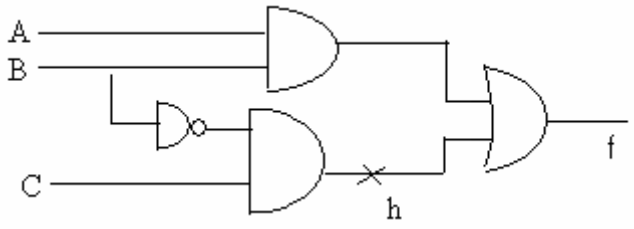

figure 2

b) Apply signature analysis to the above circuit and generate the signatures using 4-bit LFSR with a feed back from 3rd flip flop. [12]

5.a) Distinguish between Mealy and Moore machines.
b) Convert the following Mealy machine into a corresponding Moore machine. [12]

Contd….2

Machine 1

Ps	Ns, Z	
	X=0	X=1
A	B,0	D,0
B	A,0	B,0
C	D,1	A,0
D	D,1	C,0

6.a) Apply PLA maximization procedure and obtain the minimized expression to be implemented on PLA. F = 2021+0022+1200

b) Obtain the minimum test vector set for the above function 'F' in question 6 (a). [12]

7.a) Explain the different types of fault models and fault types in a PLA.

b) Plot the following PLA on the map. Identify the undetectable faults. Determine a minimal test set for detectable faults. [12]

x_1	x_2	x_3	x_4	Z_1	Z_2
0	2	2	1	1	0
2	1	1	2	1	1
0	1	2	1	0	1

8.a) The output Z of a fundamental-mode, two input sequential circuit is to change from 0 to 1 only when 2x changes from 0 to 1 while1x=1. The output is to change from 1 to 0 only when 1x changes from 1 to 0 while 2x=1.

(i) Find a minimum-row reduced flow table, the output should be fast and flicker-free.

(ii) Show a valid assignment and write a set of (static) hazard-free excitation and output equations.

b) Define the races and cycles in sequential circuits. [12]

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